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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,051	03/12/2001	Salman Akram	MIO 0069 PA	7513

7590 06/13/2006

Killworth, Gottman, Hagan & Schaeff, L.L.P.
One Dayton Centre, Suite 500
Dayton, OH 45402-2023

EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,051	AKRAM ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6-8,25-36,47,49-51,53-58 and 60-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6-8,25-36,47,49-51,53-58 and 60-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/11/05,2/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 6/26/03*.

DETAILED ACTION

This office action is in response to applicant's amendment filed October 25, 2005.

Terminal Disclaimer

The terminal disclaimer filed on January 23, 2006 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 6-8, 25-36, 47, 49-51, 53-58 and 60-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098) in combination Suzuki et al (US 5,532,910).

Lo (Fig. 1) discloses:

(cl. 2, 6, 8, 26, 28, 35, 36, 57) a first [*alternate second* for cl. 8, 31] semiconductor die (26) having a first active surface (i.e. top portion), said first active surface including at least one conductive bond pad (32); a second [*alternate first* for cl. 8] semiconductor die (40) defining a second active surface (i.e. bottom surface), said second active surface including at least one conductive bond pad (40a); a single intermediate substrate (12) comprising a network of conductive contacts (18) formed thereon, said substrate positioned between said first and second die, such that a first surface

[*alternate second* for cl. 8] of said intermediate substrate (bottom) faces said first active surface and such that a second [*alternate first* for cl. 8] surface (top portion) of said intermediate substrate faces said second active surface (bottom portion), said intermediate substrate includes a passage (defined by item 24) and one of the first and second die active surface aligned with the passage (i.e. die, 26), a printed circuit board (100) positioned such that a first surface (i.e. top portion) of the board faces the intermediate substrate; a plurality of topographic contacts (48) extending from said intermediate substrate to said first surface of said board;

(cont. cl. 8, 25) wherein said first die is electrically connected to the intermediate substrate by a topographic contact (52) extending form said first active surface to said intermediate with said second die secured (34) to the second surface of the intermediate substrate, such that the conductive pads (32) of the second die is aligned with the passage and said second die is electrically connected to the intermediate substrate by at least one conductive line (38) extending form the bond pad of the second die through said passage and to contact first surface of the intermediate substrate;

(cl. 27, 29) and the second/ *first* chip (40, 42) is flip is stacked secured to first surface of intermediate substrate (22);

(cl. 30-32) with conductive lines extending from pad (14) on the intermediate substrate to pads on active areas (i.e. chip connection to pads by pads/ or wire);

(cl. 33) die further electrically connected to intermediate substrate (i.e. chip connection to pads by pads/ or wire);

(cl. 34) and the first die is electrically connected to the second die (i.e. both in communication with external contact, 48);

(cl. 54, 55) with the intermediate substrate includes a network of contacts formed thereon (i.e. 14);

(cl. 63) a passage substantially free of encapsulant (e.g. intermediate structure prior to chip being enveloped by encapsulant; Col. 4, Lines 9-20).

Lo does not discloses at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, or a topographic contact.

Suzuki utilizes a decoupling capacitor accommodated in a space coupled to a die Suzuki (Col. 1, Lines 48).

It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor into the modified package including Lo in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

With respect to the placement of the capacitor, such that a thickness dimension of said decoupling capacitor accommodated in a space defined by a thickness dimension of one of said first semiconductor[1], it would have been obvious, since the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results. *See e.g. In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (claims held unpatentable because shifting the position of the starting switch would not

have modified the operation of the device); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

With respect to the claims 7, 49 and 50 and their dependents regarding the mere duplication of an element (i.e. intermediate substrate), since applicant has not disclosed that the duplication is for a new and unexpected result, the limitation has no patentable significance. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) (Although the reference did not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced).

Response to Arguments

Applicant's arguments filed October 20, 2005 have been fully considered but they are not persuasive[1]. Applicant contends that the Suzuki does not show coupling first or second chips, because it shows capacitors bonded to a lead frame. Examiner disagrees. A capacitor bonded to a lead frame, and capacitor coupled to a chip is not mutually exclusive. Because a chip that is connected to a lead frame that is also connected to a capacitor allows for a current to flow from the chip through the lead frame to the capacitor, it encompasses being coupled.

[1] Other than the rejection based on a commonly owned patent that has been withdrawn based on applicant's filing of a terminal disclaimer.

Applicant attempts to establish criticality for the placement of his capacitors; however, his position is moot since there is no claim reciting that the capacitor is placed between high and low voltage inputs of a die.

Lastly applicant contends that there is no expectation of success, because while Suzuki teaches to prevent noise their invention does not disclose electric noise. Examiner disagrees. Since the incorporation of capacitors in chip packages are known to improve electrical performance as indicated for example in Lin (U.S 6,849,942)[2] and eliminate noise as cited Suzuki, one of ordinary skill in the art would indeed find it reasonable to incorporate chips and capacitors with an expectation of success[3]. Furthermore the fact that applicant has recognized another advantage outside of noise, which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). For the reasons stated supra, Examiner's rejection is deemed proper and applicant's arguments found unpersuasive.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

[2] Included in IDS submitted by applicant.

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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[3] For example several references cited establish likelihood of success, that the incorporation of chip with

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Jmm
June 11, 2006

capacitors do not destroy function of chip.